

ELECTRICAL ENGINEERING DEPARTMENT  
EEL 101 FUNDAMENTALS OF ELECTRICAL ENGINEERING  
MINOR TEST - II

Date: October 14, 2008

Time: 1:00PM to 2:00PM

Max. Marks: 20

*Don't forget to write your Name, Entry No. and Group No. on your answer script.*

Q1. Given that under steady state, the two loop equations for an RLC circuit at  $\omega = 1000$  rad/sec are given by

$$\begin{array}{rclcl} \text{Loop 1} & 1I_1 & - (3 + j4)I_2 & = & V_1 = 15 \angle 45^\circ \\ \text{Loop 2} & - (3 + j4)I_1 & + (3 - j1)I_2 & = & V_2 = 0 \end{array}$$

- Draw the circuit corresponding to the set of Loop equations given above. (2)
- Find the value of  $I_1$  from the circuit drawn. (2)
- What is the power factor of the circuit as seen by the voltage source? (2)
- What would you add to the circuit to increase the power factor. (1)

Q2. In the circuit given in Fig. Q2, the switch S is in position 'a' for a long time. At time  $t = 0$ , the switch is shifted to the position 'b'.

- Identify the current  $i$  through the inductor and its derivative  $di/dt$  at time  $t = 0^+$ . Given that  $I = 2A$  and  $L = 0.5H$ ,  $R_1 = R_2 = 2\Omega$  and  $C = 1F$ .
- Find out the steady state current flowing in the inductor for  $v_m = 5 \sin 3t$ .
- Evaluate the complete response for the current through the inductor  $i(t)$ .

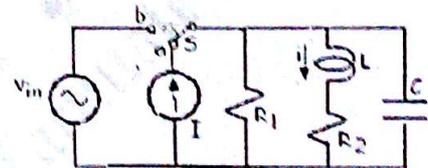


Fig. Q2

(2+1+3)

Q3. A three phase wye connected supply with a phase voltage of  $400/\sqrt{3}$  V delivers  $20/\sqrt{3}$  kW at 0.8 power factor to a delta connected balanced load. Evaluate the phase current in the balanced Delta connected load. (3)

Q4. Fig. Q4(a) gives a voltage quadrupler given in the assignment sheet distributed. The reference point at the output is not the same as the input, in other words the output is not with reference to ground. An alternate circuit is given in Fig. Q4(b) which obtains a quadrupled output with reference to ground. The four boxes marked A, B, C and D together contain a capacitor and three diodes. Identify the elements in the boxes A, B, C and D and the direction of connection of the diodes. (4)

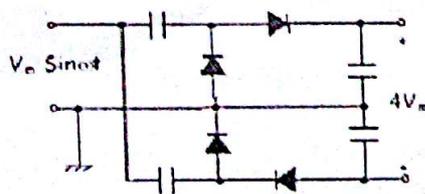


Fig. Q4(a)

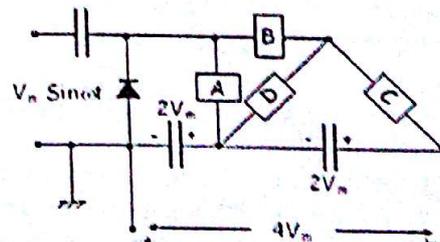


Fig. Q4(b)

GOOD LUCK ---- DO WELL